Course Syllabus

Computer Architecture

Amirkabir University of Technology
Department of Computer Engineering

Course Title:	Computer Architecture
Instructor:	Dr. Ahmad Shabani
Position:	Assistant Professor
University:	Amirkabir University of Technology
Department:	Department of Electrical Engineering
Course Level:	Undergraduate
Language of Instruction:	English / Persian
Main Focus:	Processor organization, RISC-V architecture, pipelining, memory hierarchy, and input/output systems

Course Description

Computer Architecture is a core course that introduces the structure, organization, and design principles of modern computer systems. The course begins with digital logic foundations and register-transfer operations, then moves toward processor organization, instruction-set architecture, single-cycle and multi-cycle processor design, pipelining, hazards, memory hierarchy, and input/output organization.

A major emphasis of the course is placed on understanding how hardware executes software, how instructions are represented and processed, and how performance is affected by architectural decisions. The course uses the RISC-V instruction-set architecture as a modern and practical framework for studying processor design.

Learning Objectives

By the end of this course, students should be able to:

- Understand the role of digital logic components in computer architecture.
- Explain register-transfer operations and basic microoperations.
- Describe the organization of a basic computer and processor datapath.
- Understand the language of the computer, including instruction formats and ISA concepts.
- Analyze and design a single-cycle RISC-V processor.
- Understand multi-cycle processor architecture and control mechanisms.
- Explain pipelined datapath design and identify pipeline hazards.
- Discuss branch prediction, exceptions, interrupts, and out-of-order execution concepts.
- Understand memory organization including SRAM, DRAM, cache, coherence, and virtual memory.
- Explain the role of input/output organization in computer systems.

Course Topics

Chapter 1	Digital Logics and Components: logic gates, combinational circuits, and sequential circuits.
Chapter 2	Register Transfer and Microoperations: arithmetic, logic, and shift microoperations; bus and memory transfer; optional introduction to VHDL.
Chapters 3–4	Basic Computer and Processor: basic computer organization, control unit, instruction cycle, and processor structure.
Chapter 5	Language of the Computer: instruction-set architecture, machine instructions, assembly-level representation, and program execution.
Chapter 6	Main Processor: single-cycle RISC-V architecture, datapath, control signals, and instruction execution.
Chapters 7–8	Multi-Cycle RISC-V Architecture: pipelined datapath and control, structural hazards, data hazards, control hazards, branch prediction, exceptions, interrupts, out-of-order processors, and optional array/vector processors.
Chapter 9	Input/Output Organization: I/O interfaces, communication mechanisms, interrupts, and system-level I/O behavior.
Chapter 10	Memory Organization: SRAM, DRAM, cache memory, cache coherency, and virtual memory.

Tentative Weekly Schedule

Week	Topic	Main Contents
1	Digital Logic Review	Logic gates, combinational circuits, sequential components.
2	Register Transfer	Register-transfer language, arithmetic microoperations, logic microoperations.
3	Bus and Memory Transfer	Bus structures, memory transfer operations, optional VHDL introduction.
4	Basic Computer Organization	Instruction cycle, registers, memory, control unit, datapath basics.
5	Basic Processor Design	Processor components, control flow, instruction execution.
6	Language of the Computer	ISA concepts, instruction formats, assembly-level execution.
7	Midterm Review and Exam	Review of Chapters 1–5 and midterm examination.
8	Single-Cycle RISC-V Processor	RISC-V ISA, single-cycle datapath, control signal generation.
9	Multi-Cycle Architecture	Multi-cycle datapath, control states, instruction execution over multiple cycles.
10	Pipelined Processor	Pipeline stages, pipelined datapath, pipelined control.
11	Pipeline Hazards	Structural hazards, data hazards, forwarding, stalls, control hazards.
12	Advanced Processor Concepts	Branch prediction, exceptions, interrupts, out-of-order execution.
13	Input/Output Organization	I/O modules, interrupts, communication with peripheral devices.
14	Memory Organization	SRAM, DRAM, cache, cache coherence, virtual memory, final review.

Assessment and Grading Policy

Assessment Component	Weight
Midterm Exam	30%
Final Exam	50%
Computer Assignments and Quizzes	15%
Class Contribution and Participation	5%

The midterm exam evaluates the foundational topics, including digital logic, register-transfer operations, basic computer organization, and instruction-set concepts. The final exam covers the entire course with emphasis on processor design, pipelining, memory hierarchy, and system organization.

Assignments, Quizzes, and Contribution

- Assignments may include analytical problems, processor design exercises, RISC-V instruction analysis, and memory hierarchy problems.
- Quizzes may be given during the semester to encourage continuous study.
- Class contribution includes attendance, active participation, technical discussion, and engagement with course activities.
- Late submission policies will be announced by the instructor during the semester.

Recommended Background

Students are expected to have basic familiarity with:

- Digital logic design
- Boolean algebra
- Basic programming
- Computer organization
- Assembly-level concepts
- Basic hardware components

Recommended References

- David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*.
- M. Morris Mano, *Computer System Architecture*.
- Andrew S. Tanenbaum and Todd Austin, *Structured Computer Organization*.
- RISC-V Foundation, *The RISC-V Instruction Set Manual*.

Course Policies

- Students are expected to attend lectures regularly and participate in discussions.
- Academic honesty is required in all assignments, quizzes, and exams.
- Collaboration in understanding concepts is encouraged, but submitted work must reflect the student's own effort.
- Any changes to the schedule, assignments, or grading policy will be announced by the instructor.